A Method to Implement Low Energy Read Operations, and Single Cycle Write after Read in Subthreshold SRAMs

Arijit Banerjee

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VLSI 6332 Project

Why did We Moved to Subthreshold Supply Voltages?

- $E_{SRAM/cyc} = \frac{1}{2} C_{eff} V_{DD}^2$

  $P_{SRAM} = \frac{1}{2} C_{eff} V_{DD}^2 f_{max}$

- Reducing Ceff is Costly in terms of design effort

- For Low frequency(in KHz) Medical Circuits, Vdd scaling to Subthreshold Voltages is Very Effective

Problems in 6T based Subthreshold Bitcells

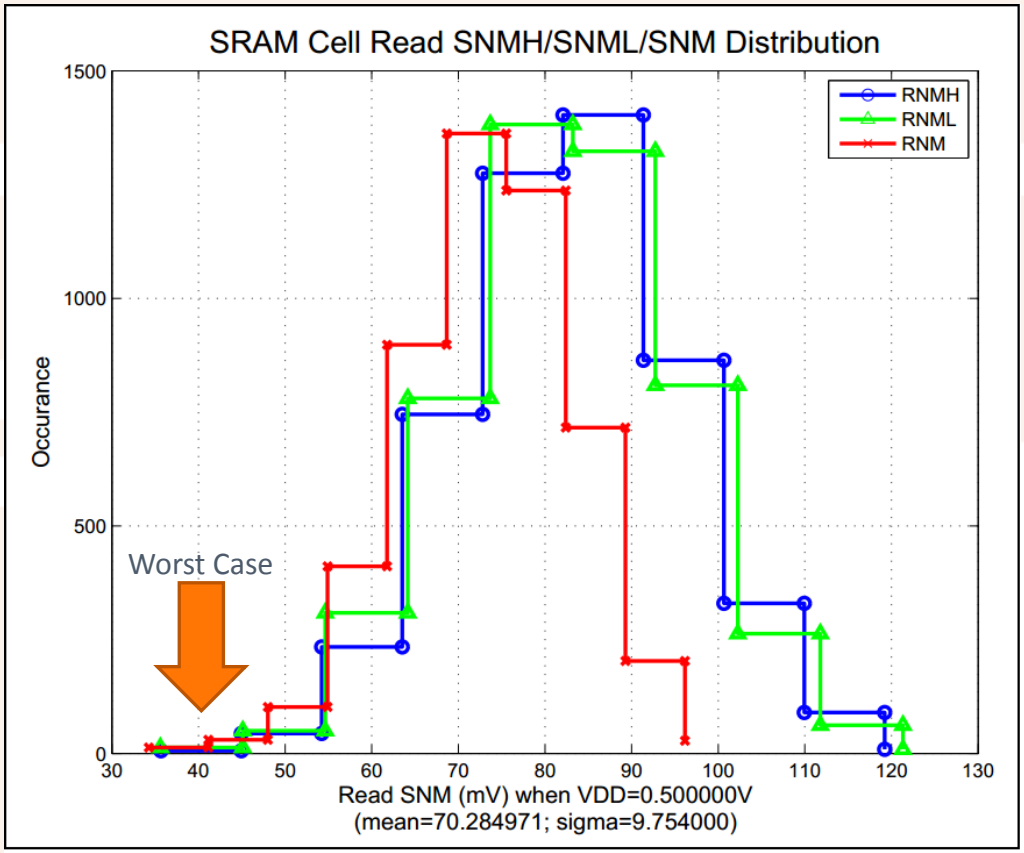
- For 6T based 8T, 9T 10T … Half select Problem in Subthreshold domain
  - Read Stress SNM in Half Selected Cells while Writing
  - No Column Muxing a must
  - Writeback (Two Cycle Write after Read) a must in Writing

How to lower Energy in 6T based Subthreshold SRAMs?

- Possibly Voltage Scaling?
  - Operating in Subthreshold Domain
  - Voltage Scaling further? Not a good Idea!
  - Vmin is Limited by Worst case RSNM, HSNM, VDRV, and so on

Minimum Operation Voltage (Vmin) Dependency

- Worse case μ - 3σ Read SNM(RSNM or RNM) for 6T

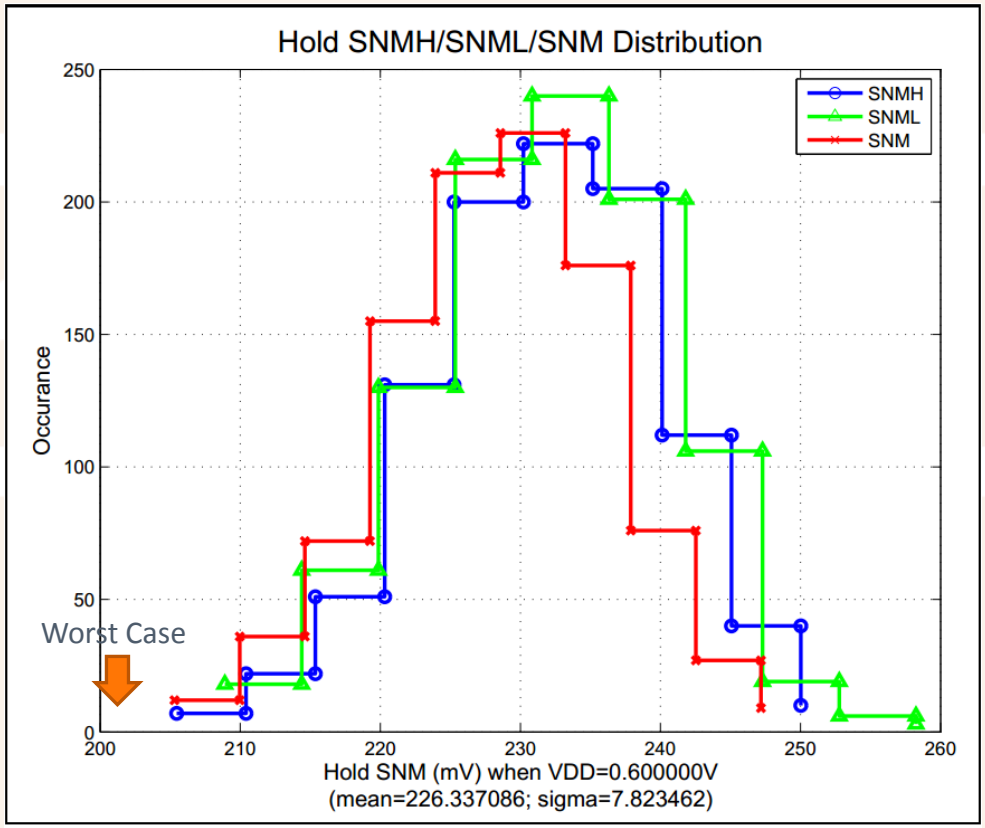


SRAM-RSNM: SRAM-RSNM

IBM 130nm data provided by James Boley BSN Chip Group @ UVa

Vmin Dependency

- Worse case μ - 3σ Hold SNM(HSNM) for 6T based 10T

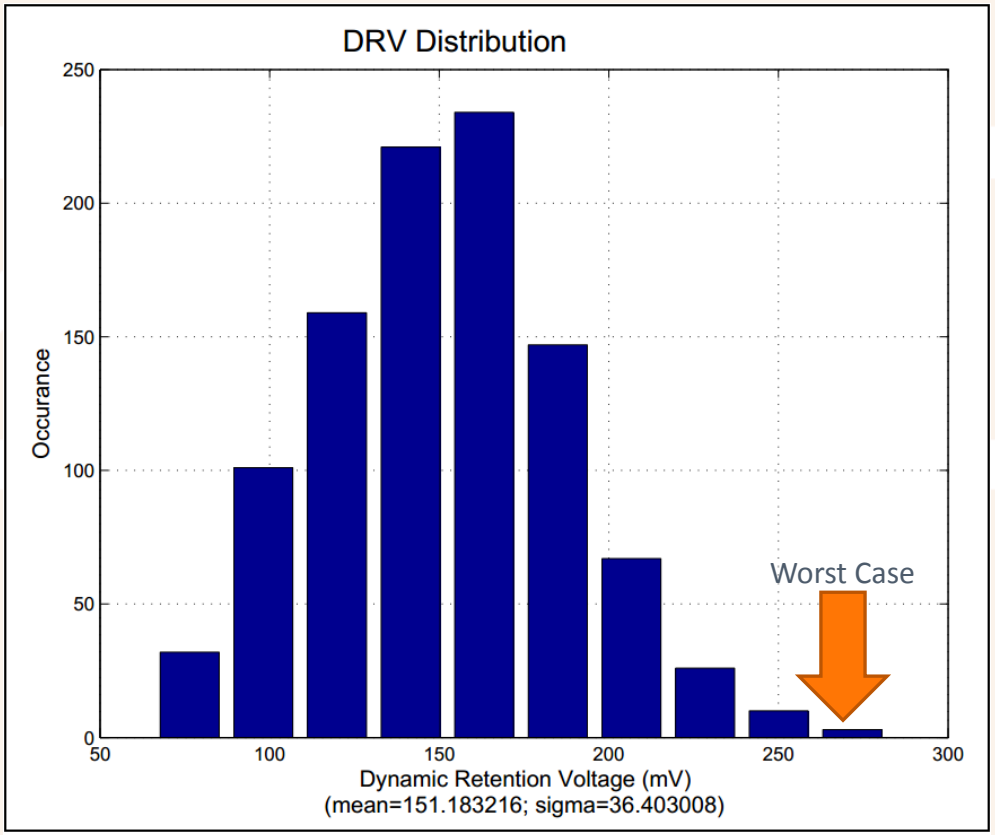


SRAM-HSNM-10T-STn: SRAM-HSNM-10T-STn

MIT 180xlp data provided by James Boley BSN Chip Group @ UVa

Vmin Dependency

- Worse case μ + 3σ Data Retention Voltage (VDRV)



SRAM-DRV-8T: SRAM-DRV-8T

IBM 130nm data provided by James Boley BSN Chip Group @ UVa

Possible Solutions to “How to lower Energy in 6T based SRAMs”

- New Type of Bitcells
- Novel Read/Write Methods
- New SRAM Architectures

Earlier Works in SRAM Dynamic Energy/Power Mitigation

Prior Work	Energy/Power Savings
Ali Valaee … SRAM Read-Assist Scheme, ISOCC, 2011	21.30%
S. Yoshimoto… Low-Energy Disturb Mitigation Scheme IEEE Symposium on VLSI Circuits Digest of Technical Papers , 2011	32%
Atsushi Kawasumi… Bitline Amplitude Limiting (BAL) Scheme, IEEE Asian Solid-State Circuits Conference on, 2011	26%
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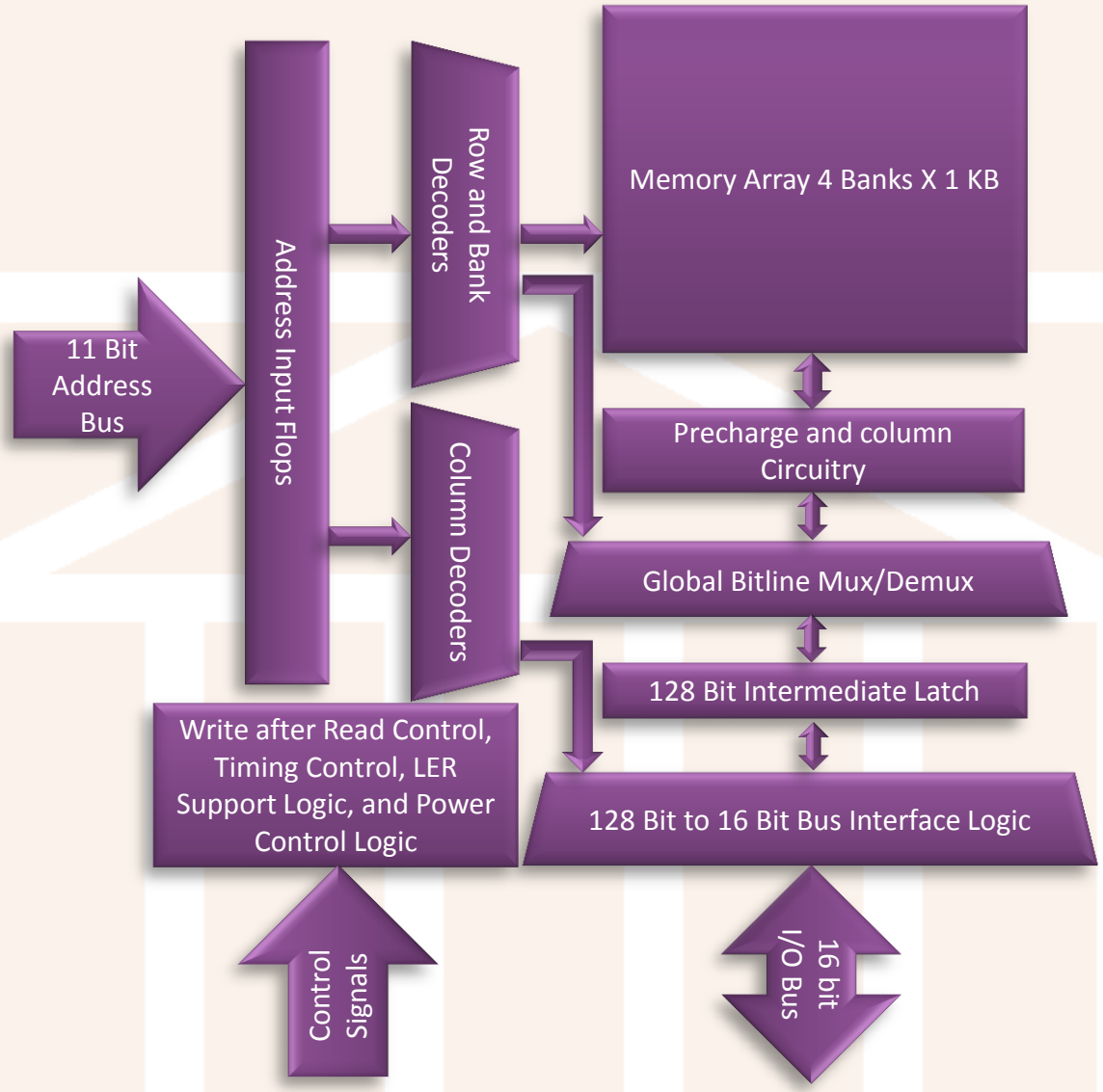
Can We do Better?

- Using RAS-CAS DRAM Timing Concept in SRAM
- Low Energy Read (LER)?
  - Do Not operate Decoders, WL Drivers
- “N-1” LER Operations per one Read in N word Row
- Auto detection of LER

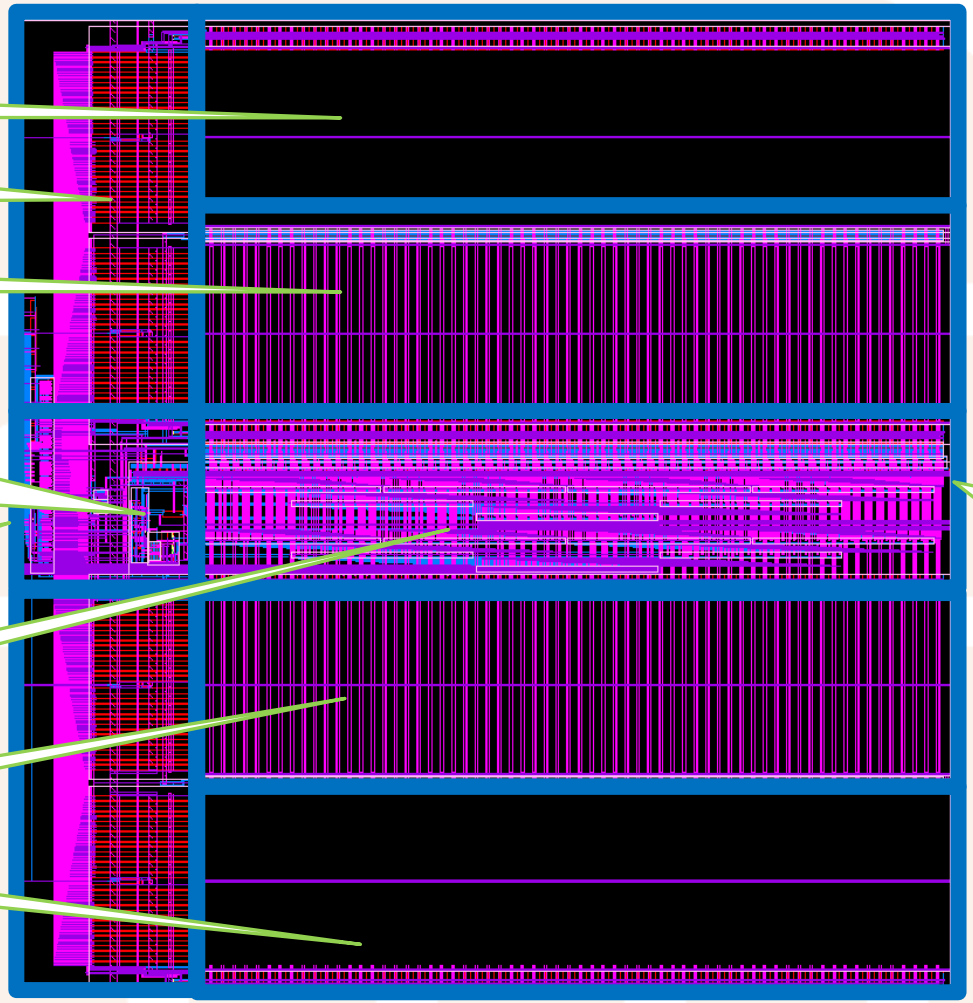
Single Cycle Write after Read(WAR)?

- Earlier Approach was Two Cycle Write after Read
- Current Approach is Single Cycle Write after Read
  - Pulsed Read and Write Word Line Generation in WAR
  - Controllable WAR Margins through External Pins
  - Using Intermediate Latch to Latch the Read Row Before Write

Block Diagram of the 4KB Subthreshold Data Memory



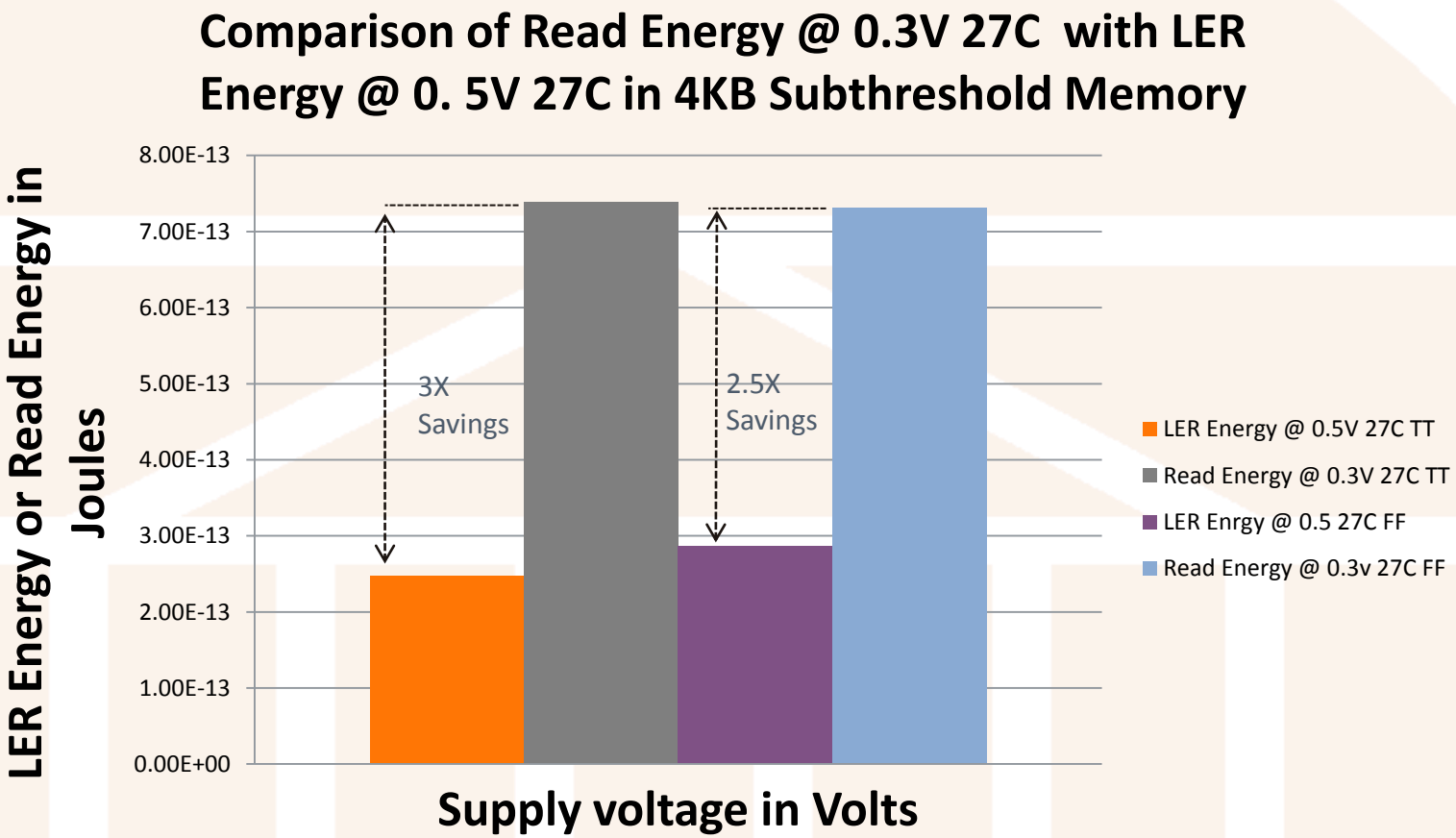
4KB Subthreshold SRAM Layout



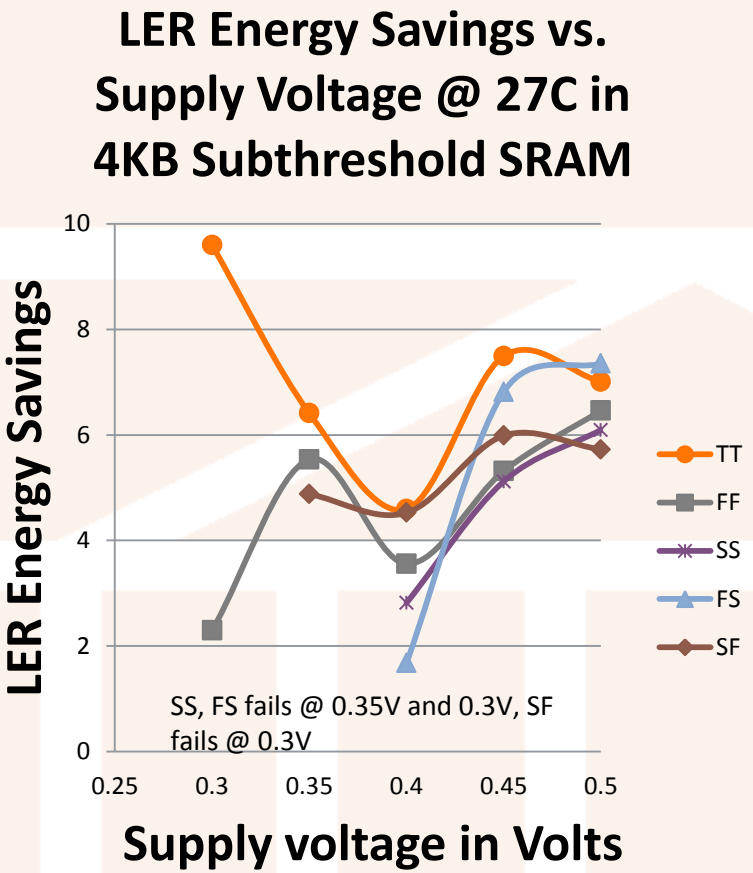
What about Half Select Problem?

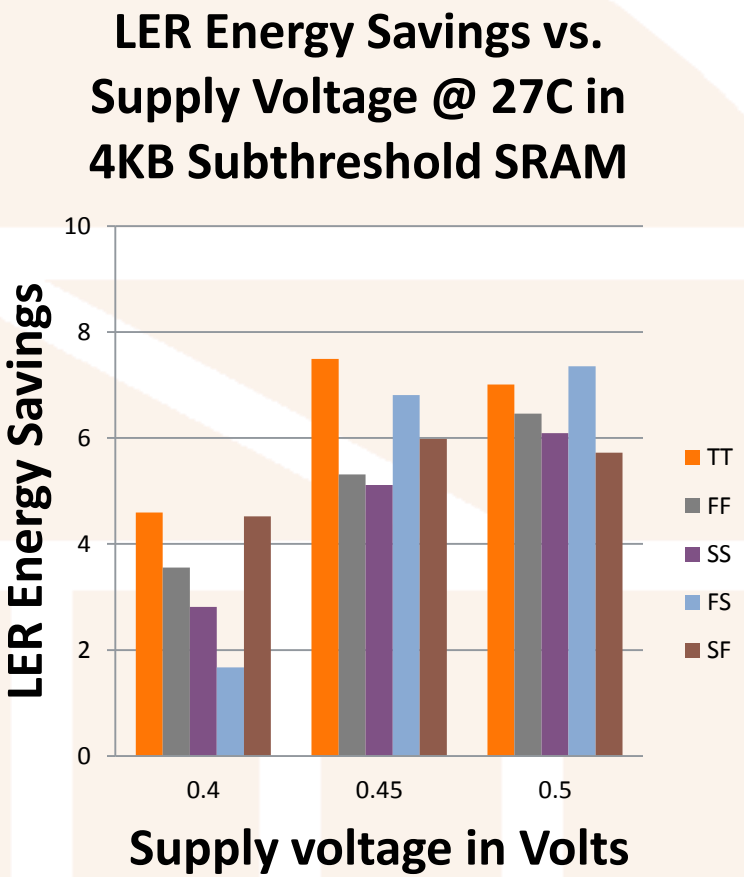
- We do not solve it; We bypass it
- No Column Mux used for avoiding half select problem
- Gains? Penalty?

Energy Comparison: Read vs. LER

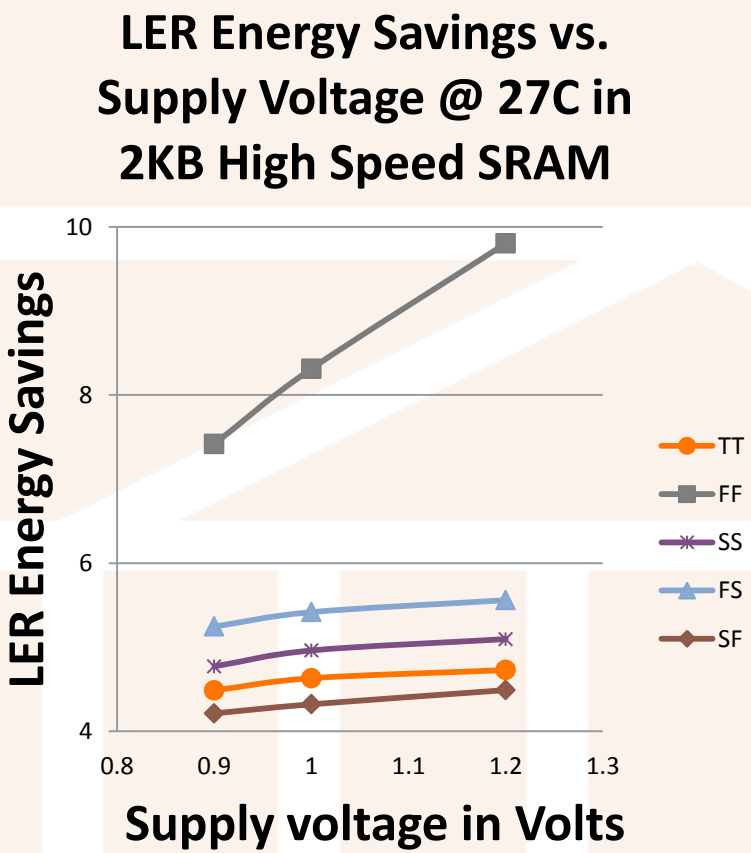


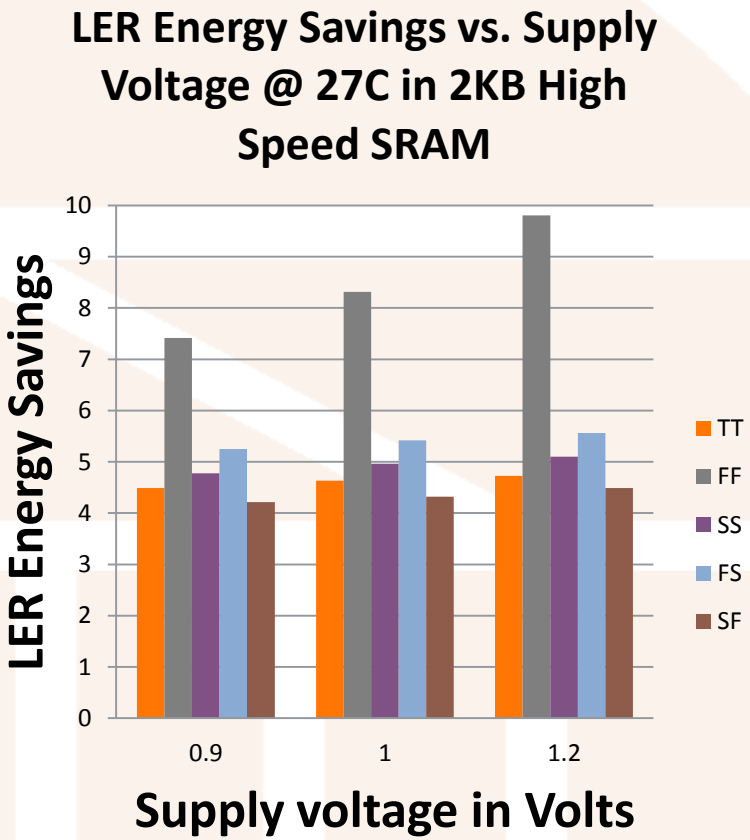
Subthreshold LER Energy Savings Trend with this Scheme



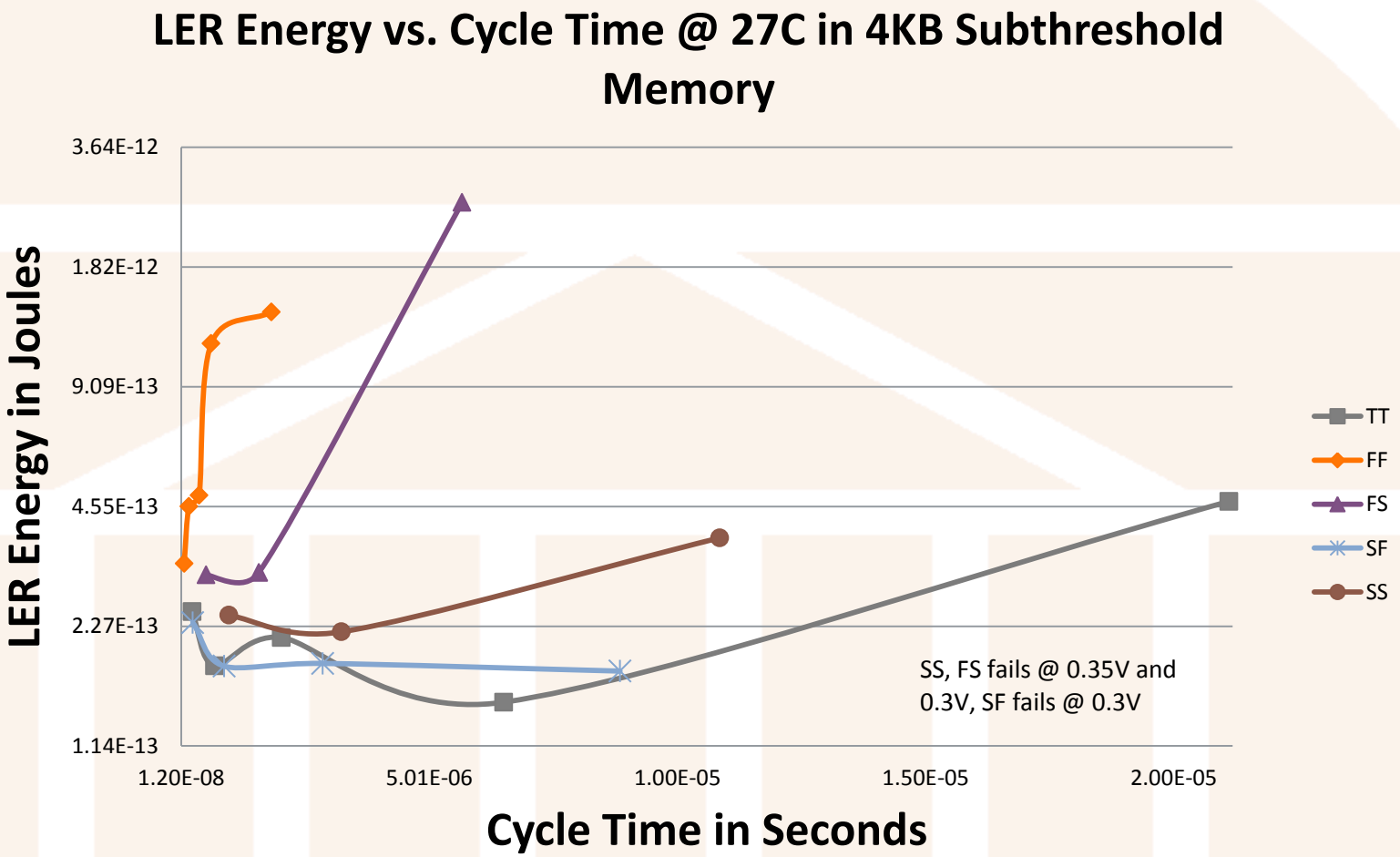


Above Subthreshold LER Energy Savings Trend

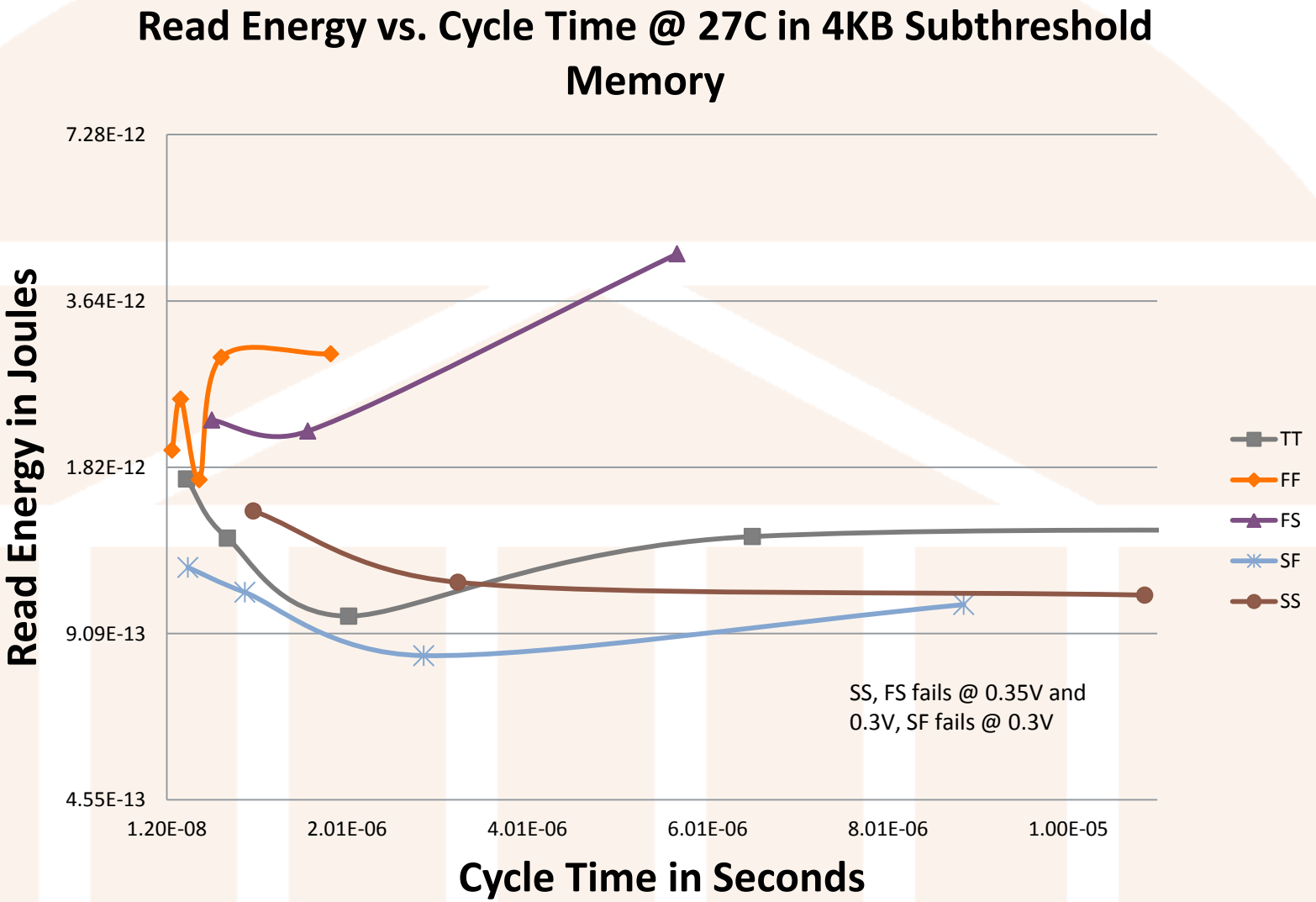




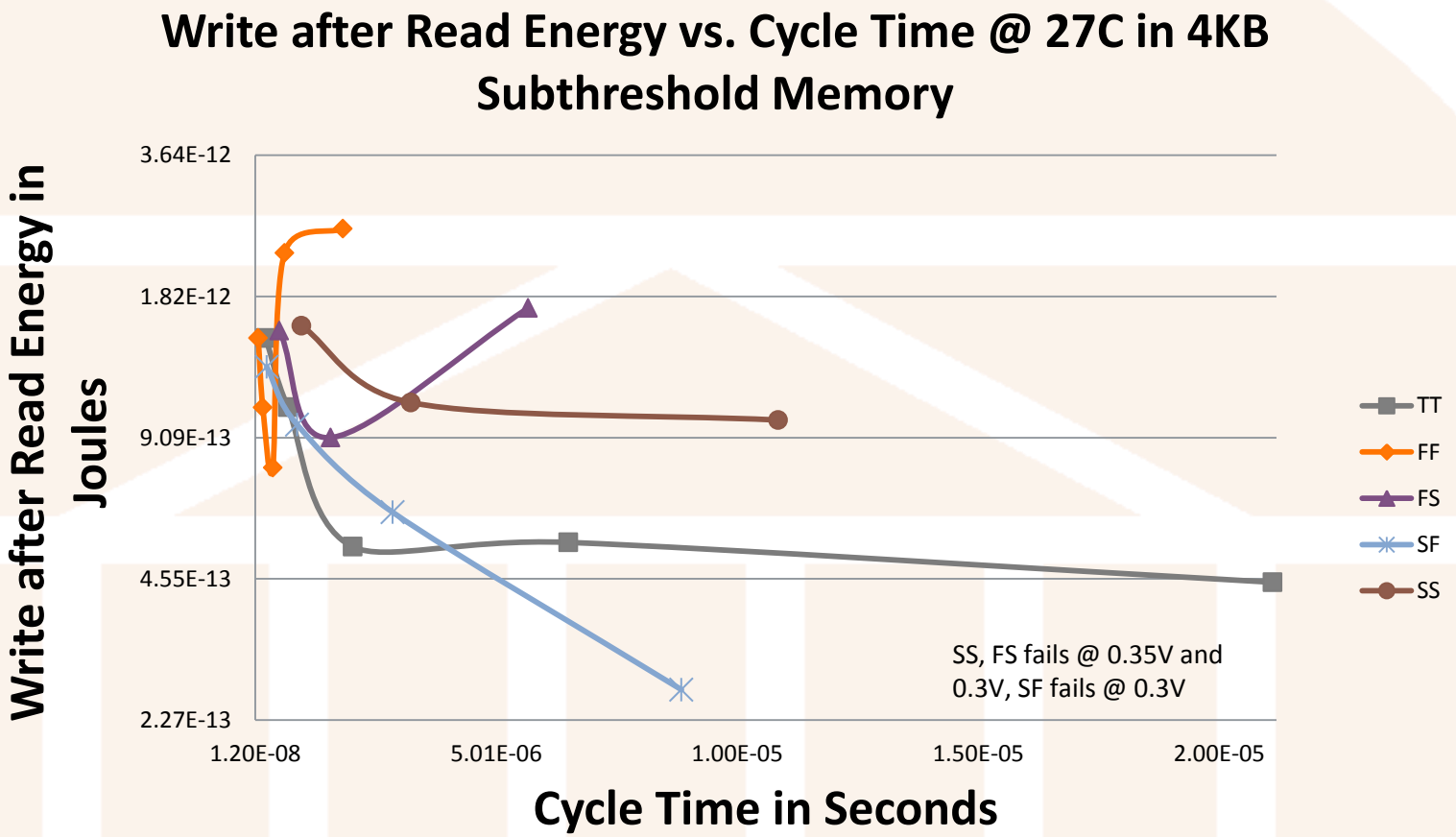
How is LER Energy vs. Cycle Time?



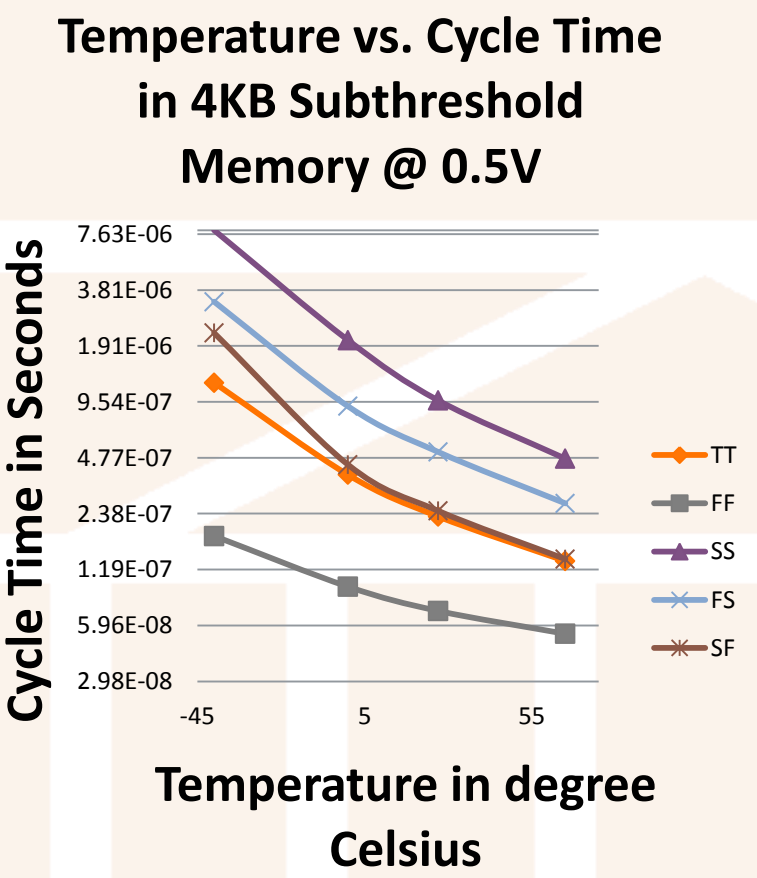
How is Read Energy vs. Cycle Time?

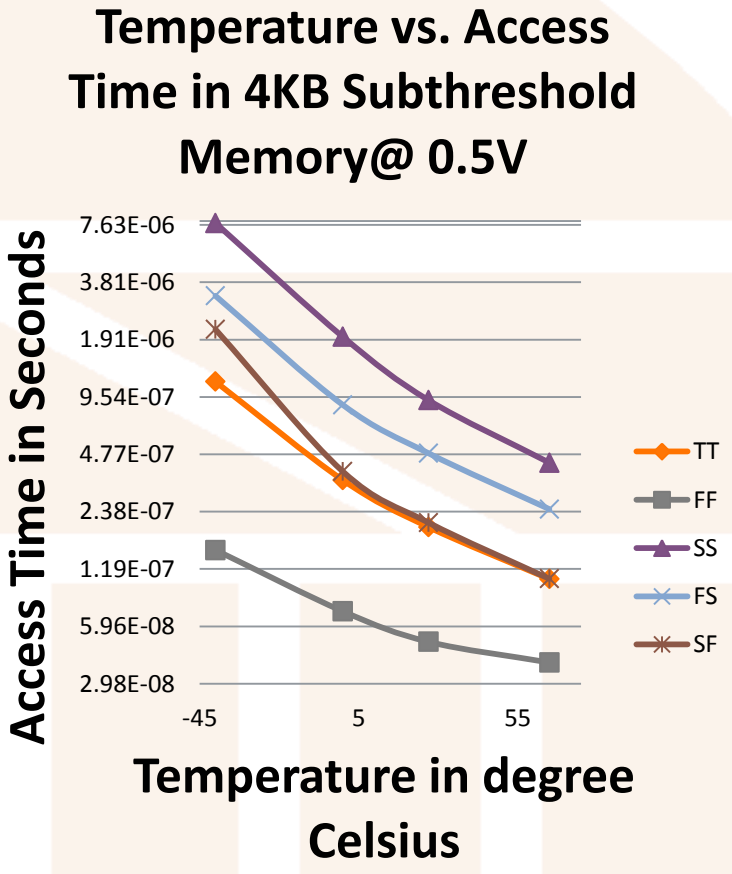


How is Write after Read Energy vs. Cycle Time?



Temperature Dependency of Cycle Time and Access Time





Comparison of Read Energy: Old vs. New Design

Processes @ 0.5V 27C	(Old Design) Average Rd Energy (in Joules)	(New Design) Average Read Energy (in Joules)		(New Design) Average LER Energy (in Joules)	
			(New Design) Rd Energy Savings		(New Design) LER Energy Savings
TT	1.74E-12	1.73E-12	1X	2.47E-13	7X
FF	1.15E-12	1.85E-12	0.6X	2.86E-13	6.5X
SS	8.21E-13	1.47E-12	0.55X	2.42E-13	6X
FS	2.39E-12	2.26E-12	1.05X	3.07E-13	7.4X
SF	7.51E-13	1.34E-12	0.56X	2.34E-13	5.7X

Comparison of Write after Read (WAR) Energy: Old vs. New Design

Processes @ 0.5V 27C	(Old Design) Average Wr + Average Rd Energy in two Cycle (in Joules)	(New Design) Average WAR or Wr Energy in one Cycle (in Joules)	Old(Wr+Rd)/new(WAR) Energy Savings
TT	2.36E-12	1.48E-12	1.6X
FF	3.12E-12	1.51E-12	2X
SS	1.30E-12	1.60E-12	0.8X
FS	3.80E-12	1.53E-12	2.5X
SF	9.76E-13	1.28E-12	0.75X

Comparison of Leakage Current: Old vs. New Design

Processes @ 0.5V 27C	(Old Design) Total Standby Leakage Current (in Amps)	(New Design) Total Standby Leakage Current (in Amps)	Leakage Savings
TT	7.05E-06	6.77E-06	1.04X
FF	2.27E-05	2.32E-05	0.97X
SS	2.55E-06	2.17E-06	1.17X
FS	1.23E-05	1.26E-05	0.98X
SF	6.90E-06	6.77E-06	1.01X

Comparison of Area and Cycle Time: Old vs. New Design

Parameters	Old Design	New Design	Gains
Area in square microns	547199.521	584920.376	-7%
Cycle Time @ TT, 0.5V,27C in nS	1401	230	6X
Access Time @ TT, 0.5V, 27C in nS	735	198	3.7X

Comparison With Prior Works

Prior Work	Energy/Power Savings
Ali Valaee … SRAM Read-Assist Scheme, ISOCC, 2011	21.30%
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This Work	5.7X @ 0.5V SF 27C, 5.1X @ 0.45 SS 27C, 1.67X @ 0.4 FS 27C

Conclusion

- 7 LER Operations per one Read in 8 word Row
- WAR Margins are Externally Controllable
- Penalty of 7% area, 3% worst case Standby Leakage, 25% worst case WAR Energy, and 45% worst case Read Energy
- Worst case 5.7X LER energy savings in KHz frequencies @ 0.5V 27C

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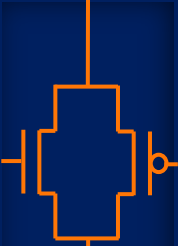

Thank You!
Questions?